CLAIMS

What is claimed is:

1. A system on a programmable chip, the system comprising:

a processor core;

a memory controller coupled to the processor core, the memory controller having a plurality of I/O lines including data, address, and control lines, the I/O lines operable to allow the processor to access off-chip tristate devices, wherein the memory controller is user configurable to either use separate sets of I/O lines for accessing off-chip tristate devices or to share one or more I/O lines for accessing off-chip tristate devices.

2. The system of claim 1, wherein one or more I/O lines shared include data and address lines.

3. The system of claim 1, wherein separate control lines are maintained even when the same set of data and address lines are shared between separate off-chip tristate devices.

4. The system of claim 3, wherein the processor is a state machine.

5. The system of claim 3, wherein the memory controller is configured automatically using a graphical configuration tool.

6. The system of claim 1, wherein I/O lines further comprise datamask lines.

7. The system of claim 1, wherein the tristate devices include SDRAM and SRAM.

8. The system of claim 7, wherein SDRAM is arranged as multiple banks of memory with independent row address management.

9. The system of claim 8, wherein the memory controller automatically maintains control of a particular SDRAM as long as back-to-back read or write transactions within the same row and bank persist.

10. The system of claim 9, wherein a break in back-to-back transactions closes a row and allows access to other tristate devices.

11. The system of claim 1, further comprising a simultaneous multiple primary component fabric coupling the processor core to the memory controller.

12. The system of claim 11, wherein the simultaneous multiple primary component fabric allows a primary component to access a secondary component while a separate primary component is accessing a separate secondary component.

13. The system of claim 12, wherein the simultaneous multiple primary component fabric comprises multiplexer coupled to the memory controller, the multiplexer operable to allow a single primary component to access the memory controller at a given time.

14. The system of claim 1, further comprising a Parallel I/O peripheral, timer, and a UART coupled to the multiple primary component fabric.

15. The system of claim 1, wherein I/O lines comprise address, data, mask, and control buses.

16. The system of claim 1, wherein the memory controller includes logic selecting one of a plurality of off-chip tristate devices for access.

17. A method for configuring a programmable chip, the method comprising:

receiving information identifying a memory controller, the memory controller associated with a processor core;

identifying a plurality of off-chip tristate devices;

receiving user configuration information through an interface to use separate sets of I/O lines or to share one or more I/O lines for accessing the off-chip tristate devices;

generating the plurality of I/O lines including data, address, and control lines to couple the memory controller with the plurality of off-chip tristate devices.

18. The method of claim 17, wherein one or more I/O lines shared include data and address lines.

19. The method of claim 17, wherein separate control lines are maintained even when the same set of data and address lines are shared between separate off-chip tristate devices.

20. The method of claim 19, wherein the processor is a state machine.

21. The method of claim 19, wherein the memory controller is configured automatically using a graphical configuration tool.

22. The method of claim 17, wherein I/O lines further comprise datamask lines.

23. The method of claim 17, wherein the tristate devices include SDRAM and SRAM.

24. The method of claim 23, wherein SDRAM is arranged as multiple banks of memory with independent row address management.

25. The method of claim 24, wherein the memory controller automatically maintains control of a particular SDRAM as long as back-to-back read or write transactions within the same row and bank persist.

26. The method of claim 25, wherein a break in back-to-back transactions closes a row and allows access to other tristate devices.

27. The method of claim 17, further comprising a simultaneous multiple primary component fabric coupling the processor core to the memory controller.

28. The method of claim 27, wherein the simultaneous multiple primary component fabric allows a primary component to access a secondary component while a separate primary component is accessing a separate secondary component.

29. The method of claim 28, wherein the simultaneous multiple primary component fabric comprises multiplexer coupled to the memory controller, the multiplexer operable to allow a single primary component to access the memory controller at a given time.

30. An apparatus for configuring a programmable chip, the apparatus comprising:

means for receiving information identifying a memory controller, the memory controller associated with a processor core;

means for identifying a plurality of off-chip tristate devices;

means for receiving user configuration information through an interface to use separate sets of I/O lines or to share one or more I/O lines for accessing the off-chip tristate devices;

means for generating the plurality of I/O lines including data, address, and control lines to couple the memory controller with the plurality of off-chip tristate devices.